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Performance Evaluation of MLI Based DVR in Grid Fed EV Fast Charging Station

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Abstract—This article proposes a power quality (PQ) solution for the compensation of voltage sag on grid fed electric vehicle fast charging stations (EVFCS) using a T-type 5-level inverter based dynamic voltage restorer (DVR). In this work, a lithium-ion battery pack with a rating of 48 V, 10 Ah, and 5 A is used as an electric vehicle (EV) battery. Firstly, the voltage sag shows a significant effect on the performance of EVFCS. The analysis of the effect of voltage sag on different characteristics of EVFCS, such as DC-bus voltage, battery current, state-of-charge (SOC), and battery voltage, is carried out in MATLAB/Simulink and through experimentation. Further, the design of the charging system is carried out using a 1- ϕ rectifier and DC-DC converter with closed loop current control. The performance of a closed loop current controlled buck converter is investigated experimentally for different magnitudes of sag (0%, 25% and 50%). Furthermore, the $\alpha\beta$ to dq transformation based synchronous reference frame (SRF) theory operated closed loop voltage controller is employed for 1- ϕ DVR to mitigate a voltage sag of 50%. This DVR maintains rated DC-bus voltage (110 V) and rated battery current (5 A) under a severe voltage sag condition of 50%. Also, DVR protects the PCC (grid) from voltage harmonics generated by the EVFCS, reducing the PCC voltage THD to 2.42% from 9.8%. Moreover, the control strategies of both the buck converter and DVR are developed on the hardware platform using the STM32 microcontroller. The simulation results are validated mathematically and experimentally. Lastly, simulation and experimental results confirm the beneficial use of T-type 5-level DVR for better performance of EVFCS.

Index Terms—Point of common coupling (PCC), multi-level inverter (MLI), electric vehicle fast charging station (EVFCS), dynamic voltage restorer (DVR), state-of-charge (SOC).

I. INTRODUCTION

NOWADAYS, the increase in pollution limits the use of internal combustion (IC) engine drives and encourages the adoption of electric vehicles (EVs), as they are environment-tally friendly. However, the EVs are facing difficulty with slow charging and disturbance of the charging process due to power quality (PQ) issues. Conventional chargers take 5 to 10 hours for full charging. Therefore, there is a need of fast charging stations for EVs. So, fast charging (2 hours) with C/2-rate is carried out in this work. The electric vehicle fast charging station (EVFCS) is either grid fed or PV fed, of which the grid fed EVFCS is considered in this article. The grid fed EVFCS is basically facing two types of problems, i.e., grid voltage quality disturbances and loading effects [1], [2]. In grid voltage quality issues, voltage sag is the major effecting disturbance. The impact of voltage sag on the performance of EVFCS is studied in this work, along with the mitigation technique of the T-type 5-level dynamic voltage restorer (DVR).

Several research studies addressed various solutions for fast charging and compensation of PQ problems in EV technology. Some of them are presented as literature reviews, as follows: A new multi-pulse flexible topology thyristor-based rectifier is presented in [3] for EV battery charging with constant current. Article [4] analysed the impact of voltage sag on grid fed EVCS; but, sag mitigation is not addressed in it. The analysis of the effect of voltage sag on an EV battery is studied in [5] along with critical voltage sag determination. However, sag mitigation and battery protection are not considered in it. In [6], the effect of loading EVs on the PV fed DC-bus is examined along with the mitigation technique employed with a supercapacitor; but, supercapacitors are not sufficient to mitigate deep voltage sag. Further, the effect of an electric vehicle's DC fast charging station on a weak AC grid is compensated in [7] using BESS. The authors in [8] proposed a new universal battery charger with a wide range of output voltages. Similarly, a single stage isolated bidirectional DC-DC converter is presented in [9] for universal EV charging. However, some topologies required ex-tra driver circuitry for fully controlled rectifiers [3], [8], [9]. A dual transformer based hybrid dual active bridge converter is proposed in [10], for plug-in EVs to cope with wide load voltages. Additionally, a single stage isolated bridgeless charger is presented in [11] for a light EV with an improved power factor; but, study of the determination of battery SOC is not carried out. In [12], a sigma modified adaptive control is studied to improve power quality in grid integrated PV for EV charging installations. Whereas, grid integrated PV based EVCS involved more power conversion stages [7], [12]. Lastly, the authors

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TABLE I
COMPARISON OF 5-LEVEL INVERTERS

Type	IGBT/ Diodes	Flying capacitors	Clamping Diodes	DC sources	DC-link capacitors
CHB	8 / 8	0	0	2	0
NPC	8 / 8	0	6	1	4
FC	8 / 8	6	0	1	4
T-type	5 / 4	0	4	1	2

in [13] analysed the sizing and scheduling of mobile energy storage systems for increasing the connectivity of RES and FCS. Moreover, very few articles in the literature have been focused on studying the impact of grid voltage quality issues on the EVFCS.

DVR is identified as the most cost effective device for the compensation of various PQ problems in the distribution system. Firstly, the effect of fault ride through capability on EVCS is studied using 3-level DVR in [14]. SMES-BES based 3-level DVR is designed in [15] to compensate voltage related issues for the sensitive load. Further, the realization of voltage sag mitigation is discussed with 1- ϕ DVR in [16]. An optimal zero-sequence voltage injection technique is introduced in [17] for 3-level DVR to mitigate asymmetric sag in a 3- ϕ 3-wire power system. In [14], [15], [17], 3-level inverter based DVR is used, which requires a larger filter circuit compared with T-type 5-level DVR. Furthermore, an enhanced SRF theory-based DVR is presented in [18] to compensate various types of voltage sags for adjustable speed drive (ASD). The authors in [19] described a dual PQ theory based DVR for compensation of voltage related PQ disturbances in the distribution system. Moreover, a new control method for a 1- ϕ 3-level dynamic voltage conditioner is introduced in [20] to compensate voltage drifts in a smart low voltage distribution system. A SMES-battery based hybrid energy storage system supported 3- ϕ 3-level DVR is used in [21] to mitigate grid voltage fluctuations. Some of the DVR topologies [15], [17], [21] cannot protect the load from deep and long duration voltage sags. Additionally, an article [22] proposed a fault ride-through technique for a DFIG wind turbine system using DVR [23]. The authors in [24] presented a fast detection method for 1- ϕ 3-level DVR with a wide range of operating conditions in a practical application. Only the 3-level DVR is used in [20], [21], [24], which requires a large filter circuit compared with the T-type 5-level VSI based DVR. Finally, graph theory based compensation of voltage sag by DVR in the distribution system is described in [25]. Hence, DVR is found to be a perfect solution to eliminate major PQD in voltage and most of the time, a two or three level inverter configuration is used for DVR. However, the MLI can be operated at a lower switching frequency, requires a relatively small size of filter, has improved performance, lower dv/dt stress across the device, and has a faster response. Therefore, in the proposed work, a reduced component T-type 5-level inverter based DVR is examined experimentally for its effectiveness in grid fed EVFCS. The T-type 5-level voltage source inverter (VSI) is selected because of its notable advantages over NPC, cascaded H-bridge (CHB), and flying capacitor (FC) MLIs [16]. The comparison of different 5-level inverters is tabulated in Table I and the comparison of different

TABLE II
COMPARISON OF SIMILAR APPROACHES

Literature	EVFCS	Effect of Sag	Sag Mitigation	Battery Protection	MLI DVR
[4]	✓	✓	×	✓	×
[5]	✓	✓	×	×	×
[14]	✓	✓	✓	✓	×
[15]	×	✓	✓	×	×
[17]	×	✓	✓	×	×
Proposed work	✓	✓	✓	✓	✓

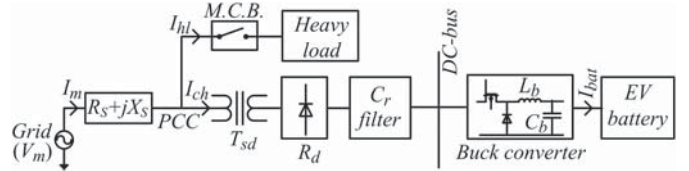


Fig. 1. Grid fed EVFCS structure.

approaches for EVFCS from the literature review is tabulated in Table II.

The novelty of this article is as follows: 1) Investigation of the effects of voltage sag on EVFCS 2) Mitigation of the effects of 25% sag using a current controlled buck converter in EVFCS 3) Mitigation of 50% voltage sag using a voltage controlled T-type 5-level DVR in EVFCS 4) Protecting the PCC (grid) from voltage harmonics generated by EVFCS using DVR.

The contribution of this article is summarised as follows: 1) A four-carrier and one-reference scheme of the PWM technique is used for T-type 5-level DVR 2) $\alpha\beta$ to dq transformation based 1- ϕ SRF controller is employed for T-type 5-level DVR 3) Implementing closed loop current control technique for buck-converter and closed loop voltage control technique for DVR 4) Protecting the battery using a charge and current controlled charging system (overcurrent protection and overcharge protection) 5) Maintaining the voltage stability of the system 6) Comparison of mitigation capability between buck converter and DVR.

The article is structured as follows: Section II described the structure and design of EVFCS with DVR. The mathematical analysis of the sag effect and DVR mitigation on EVFCS is formulated in Section III. Sections IV and V explained the control strategies of the EV charger and DVR respectively. The simulation and experimental study on EVFCS are presented in Sections VI and VII respectively. Section VIII focused on the harmonic study of EVFCS. The results are discussed in Section IX, and Section X presented concluding points.

II. DESIGNING OF EVFCS WITH DVR

The structure of grid fed EVFCS is depicted in Fig. 1. The voltage source (V_m) is connected to the PCC by source impedance (Z_s). At PCC, the step-down transformer (T_{sd}) is connected, which is input to the diode rectifier (R_d). The DC bus is formed as the output of the rectifier, which is input to the buck converter. The DC-bus voltage (V_{dc}) is high enough to provide good dynamic control. To get a 110 V DC-bus under loading

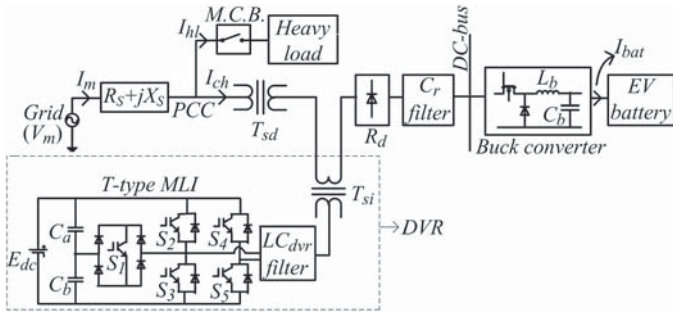


Fig. 2. T-type 5-level inverter based DVR in grid fed EVFCS structure.

TABLE III
SWITCHING STATES OF T-TYPE 5-LEVEL INVERTER

S_1	S_2	S_3	S_4	S_5	Output Voltage
0	1	0	0	1	$+E_{dc}$
1	0	0	0	1	$+E_{dc}/2$
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	0	$-E_{dc}/2$
0	0	1	1	0	$-E_{dc}$

conditions, the step-down transformer considered is 230/110 V. Further, the rectifier filter capacitor (C_r) maintains the ripple free DC-bus voltage. The combination of the rectifier, buck converter with charge and current control techniques forms an EV charger. The sag in the PCC voltage is created by switching-ON a heavy load of 2 kW connected to the PCC through a circuit breaker. This PCC voltage sag causes a sag in the rectifier input voltage without DVR mitigation. This sagacious input voltage of the rectifier causes a dip in the DC-bus voltage and charger output current. The current controlled buck converter always tries to adjust its output voltage by changing the duty cycle from 5% to 95%, so that it maintains a constant current. However, for severe sag, the buck converter is not able to produce constant output current, though it is operated at a maximum duty cycle of 95%. Hence, DVR is used in this work for mitigation of severe voltage sag on EVFCS to maintain rated DC-bus voltage and battery current.

The DVR connected EVFCS structure is shown in Fig. 2. The DVR consists of a VSI, a DC energy storage system, an LC filter, and a series injection transformer (T_{si}). The DVR has to inject voltage with enough amplitude, frequency and in-phase with the transformer's output voltage. The DVR is bridged in the middle of the step-down transformer and diode rectifier using a series injection transformer. During voltage sag, the DVR injects voltage in series with the transformer output voltage to maintain the sag free input voltage of the rectifier. A T-type 5-level inverter is used as the VSI of the DVR. The switching states to produce 5-level output for the T-type 5-level inverter are tabulated in Table III. A four-carrier and one-reference scheme generates the required gate pulses in simulation, as depicted in Fig. 3. The real time gate pulse generation is shown in Fig. 4, in which g_1 , g_2 , g_3 , g_4 are captured in 4-channel DSO, and g_5 is inverse to g_4 . Further, the 5-level output of the T-type inverter is shown in Fig. 5. The system specifications of the EVFCS are tabulated in

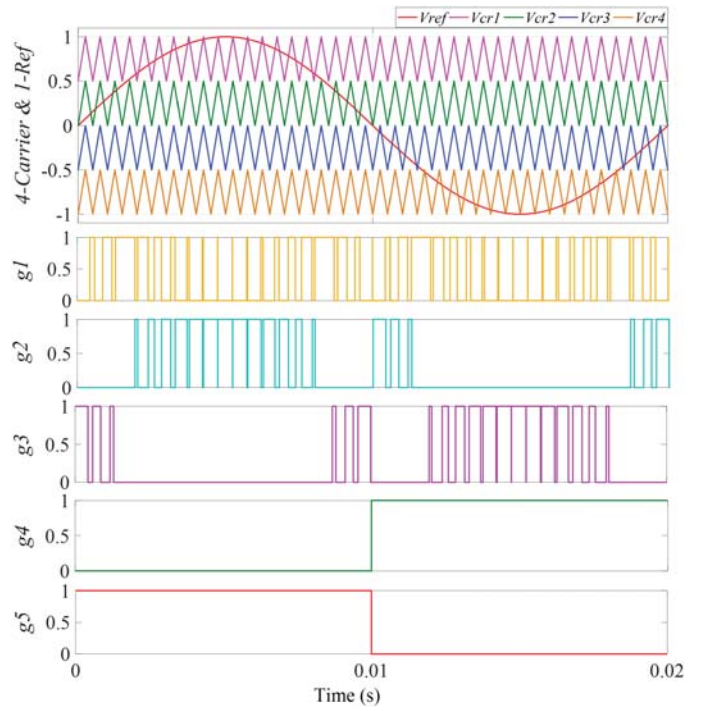


Fig. 3. Gate pulse generation of T-type 5-level inverter in simulation.

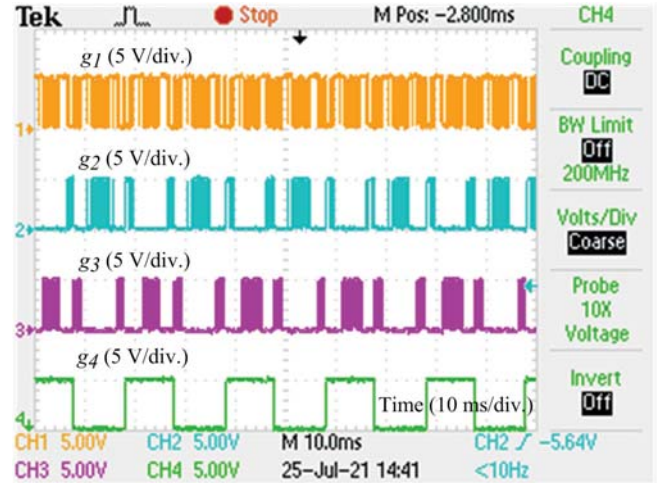


Fig. 4. Gate pulse generation of T-type 5-level inverter in hardware.

Table IV. The DC-bus voltage (V_{dc}) is calculated as

$$V_{dc} = 1.414V_{ri} \quad (1)$$

where V_{ri} is rectifier input voltage

The rectifier filter capacitor (C_r) is calculated as

$$C_r = \frac{P_{dc}}{4\pi f_m V_{dc} \Delta V_{dc}} \quad (2)$$

where f_m is mains frequency (50 Hz), P_{dc} is the rated DC power, ΔV_{dc} is ripple output voltage of rectifier.

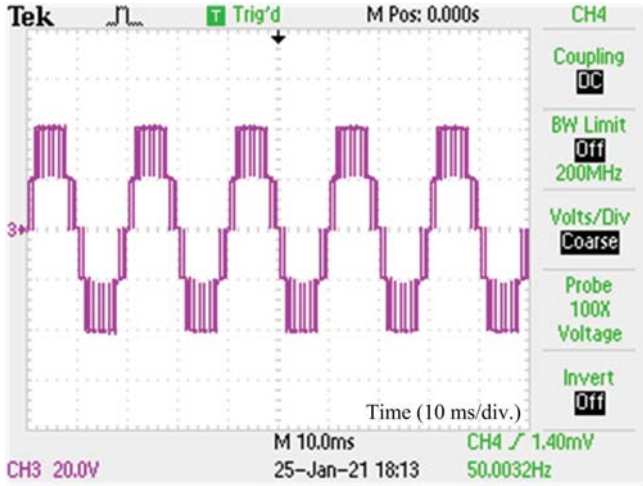


Fig. 5. 5-level output of T-type 5-level inverter in hardware.

TABLE IV
SYSTEM SPECIFICATIONS OF EVFCS

System	Specification	Valuation
Supply	Voltage (V_m)	230.0 V
	Step-down transformer (T_{sd})	1000 VA, 230/110 V
	Duration of sag	0.4 to 0.6 s
	Impedance ($Z_s = R_s + jX_s$)	2.0 Ω
	Heavy load	230 V, 2 kW
Buck-converter	Filter inductor (L_b)	3e-3 H
	Filter capacitor (C_b)	1000e-6 F
	Switching frequency (f_{sb})	20 kHz
	k_{Pb} and k_{Ib}	0.5, 0.3
	MOSFET	IRFP460N
Rectifier	Filter capacitor (C_r)	4400e-6 F
Battery	Ah rating	10 Ah
	Voltage (V_{bat})	48 V
	Battery current (I_{bat})	5 A
DVR	Filter inductor (L_{dvr})	1e-3 H
	Filter capacitor (C_{dvr})	42e-6 F
	Injection Transformer (T_{si})	1000 VA, 110/110 V
	Input of T-type MLI (E_{dc})	80 V
	Switching frequency (f_{sdvr})	2 kHz
	k_{Pdvr} and k_{Idvr}	0.1, 0.01
	IGBT	FGA25N120
	Diode	10A10 MIC

The buck filter capacitor (C_b) is calculated as

$$C_b = \frac{\Delta I_L}{8f_{sb}\Delta V_{bat}} \quad (3)$$

where ΔI_L is ripple current, ΔV_{bat} is ripple output voltage of buck-converter, f_{sb} is switching frequency of buck converter (20 kHz).

The inductor of buck converter (L_b) is calculated as

$$L_b = \frac{V_{bat}(V_{dc} - V_{bat})}{V_{dc}f_{sb}\Delta I_L} \quad (4)$$

The DVR filter capacitor (C_{dvr}) is calculated as

$$C_{dvr} = \frac{100}{4\pi^2 f_{sdvr}^2 L_{dvr}} \quad (5)$$

where f_{sdvr} is switching frequency of DVR (2 kHz)

The DVR filter inductor (L_{dvr}) is calculated as

$$L_{dvr} = \frac{E_{dc}}{4f_{sdvr}\Delta I_L} \quad (6)$$

where E_{dc} is input of T-type 5-level inverter.

The VA rating of DVR (S_{dvr}) is calculated as

$$S_{dvr} = V_{dvr}I_{dvr} \quad (7)$$

where V_{dvr} is the voltage injected by the DVR, I_{dvr} is the current flowing through the DVR.

III. STUDY OF SAG EFFECT AND MITIGATION USING DVR ON EVFCS

A. Effect of Voltage Sag on EVFCS

1) *Output Voltage of Transformer:* The PCC delivers its output as input to the step-down transformer (V_{ti}). The transformer output voltage (V_{to}) relates with PCC voltage (V_p) as follows

$$V_m - V_d = V_p = V_{ti} \quad (8)$$

$$V_{to} = kV_{ti} \quad (9)$$

using (8) in (9)

$$V_{to} = kV_p \quad (10)$$

where V_m is the supply voltage, V_d is drop due to source impedance and k is ratio of transformation.

2) *Rectifier Output Voltage:* The transformer delivers its output (V_{to}) as input to the rectifier (V_{ri}).

$$V_{to} = V_{ri} \quad (11)$$

using (11) in (1)

$$V_{dc} = 1.414V_{to} \quad (12)$$

using (10) in (12)

$$V_{dc} = 1.414kV_p \quad (13)$$

3) *Battery Voltage:* The rectifier delivers its output (V_{dc}) as input to the buck converter (V_{dc}). The sag effected battery voltage (V_{bat}) is

$$V_{bat} = \alpha V_{dc} \quad (14)$$

using (13) in (14)

$$V_{bat} = 1.414\alpha kV_p \quad (15)$$

where α is the duty cycle of buck converter.

4) *Battery Current:* The sag effected battery current is

$$I_{dc} = \alpha I_{bat} \quad (16)$$

$$I_{bat} = \frac{V_{bat}}{R_{bat}} \quad (17)$$

using (15) in (17)

$$I_{bat} = \frac{1.414\alpha kV_p}{R_{bat}} \quad (18)$$

where R_{bat} is the battery resistance, I_{dc} is DC-bus current

5) *Battery SOC*: Sag effected charge of the battery (Q_{bat}) is

$$I_{bat} = \frac{dQ_{bat}}{dt} \quad (19)$$

using (18) in (19)

$$\frac{dQ_{bat}}{dt} = \frac{1.414\alpha kV_p}{R_{bat}} \quad (20)$$

B. Effect of DVR Compensation on EVFCS

1) *Rectifier Output Voltage*: The input of rectifier (V_{ri}) is the addition of DVR injected voltage (V_{dvr}) and output of transformer (V_{to}).

$$V_{to} + V_{dvr} = V_{ri} \quad (21)$$

The DVR's injected voltage depends on the modulation index (MI) where it is operated. However, the MI should depend upon the P.U. sag (x). In this work, the DVR is designed to mitigate 50% voltage sag. In order to maintain the THD of the DVR voltage less, it has to operate with a high MI. For 50% voltage sag, x becomes 0.5. However, if the DVR is operated with MI at 0.5, the same as with x , then it will inject voltage with more harmonics. This is the reason the MI is considered as $2x$, so as to operate the DVR with MI as 1 for less THD in the output voltage.

$$V_{dvr} = \frac{E_{dc}}{1.414} MI \quad (22)$$

Substituting MI as $2x$ in (22)

$$V_{dvr} = \frac{E_{dc}}{1.414} 2x = 1.414x E_{dc} \quad (23)$$

using (21) in (1)

$$V_{dc} = 1.414(V_{to} + V_{dvr}) \quad (24)$$

using (10) and (23) in (24)

$$V_{dc} = 1.414(kV_p + 1.414x E_{dc}) \quad (25)$$

where x is sag in P.U. and E_{dc} is input voltage of T-type 5-level inverter.

2) *Battery Voltage*: The effect of DVR compensation on buck output voltage is

using (25) in (14)

$$V_{bat} = 1.414\alpha(kV_p + 1.414x E_{dc}) \quad (26)$$

3) *Battery Current*: The buck output current is delivered as battery current and its compensation using DVR is

using (26) in (17)

$$I_{bat} = \frac{1.414\alpha(kV_p + 1.414x E_{dc})}{R_{bat}} \quad (27)$$

4) *Battery SOC*: The sag mitigated charge of the battery is as follows

using (27) in (19)

$$\frac{dQ_{bat}}{dt} = \frac{1.414\alpha(kV_p + 1.414x E_{dc})}{R_{bat}} \quad (28)$$

C. Sensitivity Analysis

The total grid current (I_m) is the sum of current drawn by heavy load (I_{hl}) and charging current (I_{ch}) from Fig. 1 as follows.

$$I_m = I_{hl} + I_{ch} \quad (29)$$

Further it can be written as

$$\frac{dI_m}{dt} = \frac{dI_{hl}}{dt} + \frac{dI_{ch}}{dt} \quad (30)$$

The act of switching-ON heavy load at the PCC and engaging in EV charging leads to voltage sag at the PCC. This is because of voltage drop takes place across source impedance due to heavy load current and EV charging current.

$$V_p = V_m - I_m R_s - L_s \frac{dI_m}{dt} \quad (31)$$

Case-1: No-load

$$V_p = V_m \quad (32)$$

Case-2: Charging mode without heavy load

$$V_p = V_m - I_{ch} R_s - L_s \frac{dI_{ch}}{dt} \quad (33)$$

Case-3: Charging mode with heavy load

$$V_p = V_m - I_{hl} R_s - I_{ch} R_s - L_s \frac{dI_{hl}}{dt} - L_s \frac{dI_{ch}}{dt} \quad (34)$$

Further, the sensitivity of PCC voltage with respect to heavy load current is

$$S_{I_{hl}}^{V_p} = \frac{\frac{\partial V_p}{\partial I_{hl}}}{\frac{I_{hl}}{I_{hl}}} = \frac{\partial V_p}{\partial I_{hl}} \frac{I_{hl}}{V_p} \quad (35)$$

The sensitivity of PCC voltage with respect to charging current is

$$S_{I_{ch}}^{V_p} = \frac{\frac{\partial V_p}{\partial I_{ch}}}{\frac{I_{ch}}{I_{ch}}} = \frac{\partial V_p}{\partial I_{ch}} \frac{I_{ch}}{V_p} \quad (36)$$

The heavy load's current draw is significantly greater than the EV charging current. Therefore, heavy load current has a more significant effect on the PCC voltage as compared with charging current. Hence, the sensitivity of PCC voltage with respect to heavy load current is greater than the sensitivity of PCC voltage with respect to charging current.

$$I_{ch} < I_{hl} \quad (37)$$

$$S_{I_{ch}}^{V_p} < S_{I_{hl}}^{V_p} \quad (38)$$

In the absence of a DVR configuration, the transformer's output voltage directly serves as the input voltage for the rectifier, resulting in a sag in the rectifier's input voltage. This reflects the DC-bus voltage not maintaining its rated value there by the entire charging process. Comparing (10) and (11)

$$V_{ri} = kV_p \quad (39)$$

Using (34) in (39)

$$V_{ri} = k \left[V_m - I_{hl} R_s - I_{ch} R_s - L_s \frac{dI_{hl}}{dt} - L_s \frac{dI_{ch}}{dt} \right] \quad (40)$$

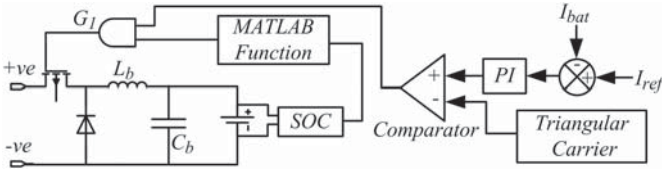


Fig. 6. Control strategy of buck converter.

substituting k and V_m values in (40)

$$V_{ri} = \frac{110}{230} \left[230 - I_{hl}R_s - I_{ch}R_s - L_s \frac{dI_{hl}}{dt} - L_s \frac{dI_{ch}}{dt} \right] \quad (41)$$

Simplifying (41)

$$V_{ri} < 110 \quad (42)$$

To get constant DC-bus voltage, it is necessary to maintain a sag free rectifier input voltage. With mitigation technique, DVR injects the same amount of voltage as that effected by heavy load current and charging current. The DVR maintains a sag free rectifier input voltage there by the constant DC-bus voltage. Using (10) in (21)

$$V_{ri} = kV_p + V_{dvr} \quad (43)$$

Using (34) in (43)

$$V_{ri} = k \left[V_m - I_{hl}R_s - I_{ch}R_s - L_s \frac{dI_{hl}}{dt} - L_s \frac{dI_{ch}}{dt} \right] + V_{dvr} \quad (44)$$

Simplifying (44)

$$V_{ri} = kV_m = \frac{110}{230} * 230 = 110 \quad (45)$$

IV. CONTROL STRATEGY FOR BUCK CONVERTER

The control strategy of the buck converter is shown in Fig. 6. In which, the reference battery current (I_{ref}) is taken as 5 A. The actual battery current (I_{bat}) is sensed and subtracted from I_{ref} . The error between I_{ref} and I_{bat} is fed to the PI controller. The linear output of the PI controller is compared with a carrier signal of 20 kHz frequency. The gate pulse for constant current control is generated using the STM32 microcontroller. Further, the SOC of the battery is obtained from the current integration method using the STM32 microcontroller. The initial SOC of the battery is measured at 50%. Both charge and current control techniques are needed for the safe and secure operation of lithium-ion batteries. A 48 V, 10 Ah lithium-ion battery takes 2 hours to charge at C/2-rate (5 A).

The hardware results show the effect of voltage sag on the performance of the buck converter as disclosed in Fig. 7. When there is no sag, the DC-bus voltage is maintained at 110 V, as shown in channel-1 of Fig. 7(a). Then the duty cycle is adjusted to almost 50% through the closed-loop current control strategy as observed in channel-2. This leads to a rated battery current of 5 A, as depicted in channel-3.

Whenever sag occurs up to 25%, the duty cycle is increased to maintain the constant buck output current through the closed-loop current control strategy as shown in Fig. 7(b). The DC bus voltage is 80 V with 25% sag, as depicted in channel-1. Then the duty cycle is adjusted to almost 75% as observed in channel-2 to draw the rated battery current of 5 A, as exhibited in channel-3.

Further, the DC bus voltage is 55 V for a severe voltage sag of 50% as depicted in channel-1 of Fig. 7(c). Then the duty cycle is adjusted to 95% through the closed-loop current control strategy as shown in channel-2. Even though the duty cycle is adjusted to 95%, the battery is taking a reduced current of 2.5 A only, as observed in channel-3. Hence, the buck converter fails to maintain constant battery current through the current control strategy with a severe voltage sag of 50%.

V. CONTROL TECHNIQUE FOR DVR

The buck converter is unable to maintain the battery's rated current in severe voltage sag conditions. Therefore, DVR mitigation is mandatory for voltage sag compensation on EVFCS. The SRF theory based control circuitry of a 1- ϕ DVR is shown in Fig. 8. It consists of the $\alpha\beta$ to dq transformation, the inverse transformation of dq to $\alpha\beta$, synchronizing 1- ϕ PLL and PI controller. Further, the DVR injects voltage with fewer harmonics as the modulation index (MI) of the T-type 5-level inverter is operated nearer to 1. The mains supply, PCC, and load voltages are sensed and fed as inputs to the control circuitry. The original 1- ϕ quantity is fed as α -component, whereas the β -component is acquired by shifting the α -component to 90° . Lastly, $V_{f\alpha\beta}$ is the error signal generation in which $V_{f\beta}$ is ignored and $V_{f\alpha}$ is processed for generating PWM technique. The PWM methodology produces gate pulses on the STM32 microcontroller. The PCC voltage (V_p) is converted to dq frame from $\alpha\beta$ shown in (46) and (47)

$$V_{pd} = V_{p\alpha} \cdot \sin \omega t - V_{p\beta} \cdot \cos \omega t \quad (46)$$

$$V_{pq} = V_{p\alpha} \cdot \cos \omega t + V_{p\beta} \cdot \sin \omega t \quad (47)$$

The rectifier input voltage (V_{ri}) is converted to dq frame from $\alpha\beta$ as shown in (48) and (49)

$$V_{rid} = V_{ri\alpha} \cdot \sin \omega t - V_{ri\beta} \cdot \cos \omega t \quad (48)$$

$$V_{riq} = V_{ri\alpha} \cdot \cos \omega t + V_{ri\beta} \cdot \sin \omega t \quad (49)$$

The mains supply voltage (V_m) is converted to dq frame from $\alpha\beta$ as shown in (50) and (51)

$$V_{md} = V_{m\alpha} \cdot \sin \omega t - V_{m\beta} \cdot \cos \omega t \quad (50)$$

$$V_{mq} = V_{m\alpha} \cdot \cos \omega t + V_{m\beta} \cdot \sin \omega t \quad (51)$$

The difference between PCC voltage (V_p) and rectifier input voltage (V_{ri}) in dq frame is shown in (52) and (53)

$$V_{ad} = V_{pd} - V_{rid} \quad (52)$$

$$V_{aq} = V_{pq} - V_{riq} \quad (53)$$

The difference between mains voltage (V_m) and rectifier input voltage (V_{ri}) in dq frame shown in (54) and (55)

$$V_{bd} = V_{md} - V_{rid} \quad (54)$$

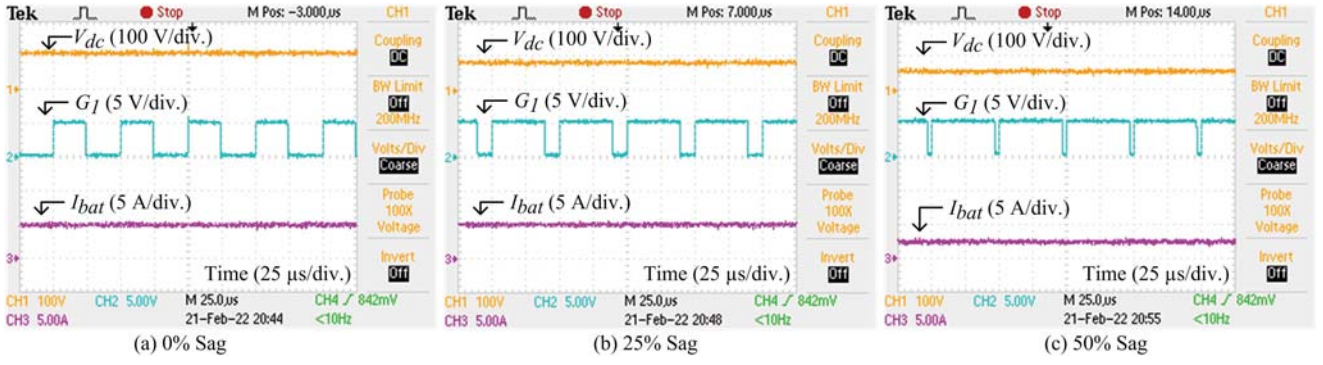


Fig. 7. Hardware results of buck converter (Ch1) DC-bus voltage- V_{dc} (Ch2) gate pulse- G_1 (Ch3) battery current- I_{bat} .

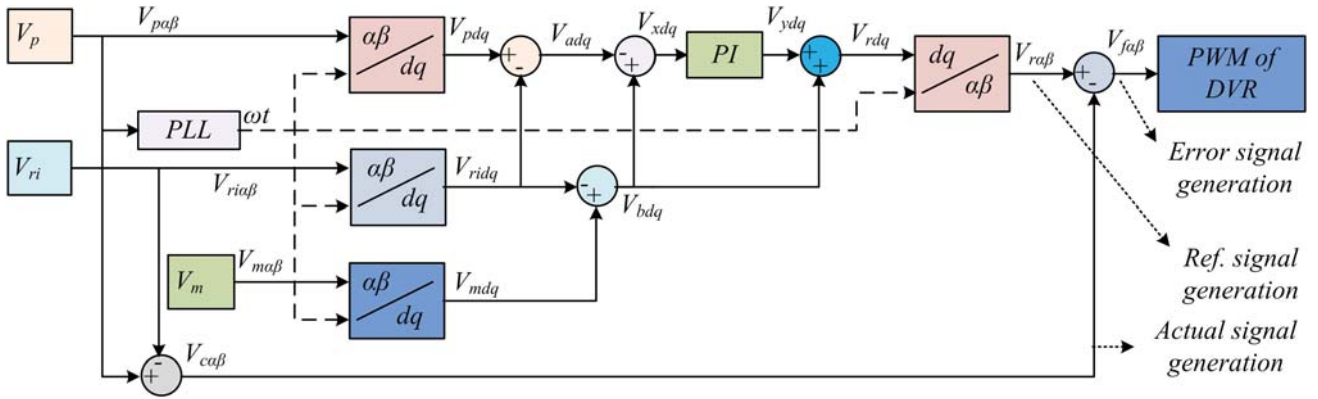


Fig. 8. SRF control scheme of 1- ϕ DVR.

$$V_{bq} = V_{mq} - V_{riq} \quad (55)$$

The difference of V_{bdq} , V_{adq} is shown in (56) and (57)

$$V_{xd} = V_{bd} - V_{ad} \quad (56)$$

$$V_{xq} = V_{bq} - V_{aq} \quad (57)$$

The PI controller output V_{ydq} relates with input V_{xdq} is as shown in (58) and (59)

$$V_{yd} = V_{xd} \cdot k_p + V_{xd} \int k_i dt \quad (58)$$

$$V_{yq} = V_{xq} \cdot k_p + V_{xq} \int k_i dt \quad (59)$$

The addition of V_{ydq} , V_{bdq} is shown in (60) and (61)

$$V_{rd} = V_{bd} + V_{yd} \quad (60)$$

$$V_{rq} = V_{bq} + V_{yq} \quad (61)$$

The reference signal ($V_{r\alpha\beta}$) generation from V_{rdq} through inverse transformation is shown in (62) and (63)

$$V_{r\alpha} = V_{rd} \cdot \sin \omega t + V_{rq} \cdot \cos \omega t \quad (62)$$

$$V_{r\beta} = -V_{rd} \cdot \cos \omega t + V_{rq} \cdot \sin \omega t \quad (63)$$

The actual signal ($V_{c\alpha\beta}$) generation is carried out in $\alpha\beta$ frame as shown in (64) and (65)

$$V_{c\alpha} = V_{p\alpha} - V_{ri\alpha} \quad (64)$$

$$V_{c\beta} = V_{p\beta} - V_{ri\beta} \quad (65)$$

The error signal ($V_{f\alpha\beta}$) generation is carried out through the difference of $V_{r\alpha\beta}$, $V_{c\alpha\beta}$ is shown in (66) and (67)

$$V_{f\alpha} = V_{r\alpha} - V_{c\alpha} \quad (66)$$

$$V_{f\beta} = V_{r\beta} - V_{c\beta} \quad (67)$$

VI. SIMULATION STUDY ON EVFCS

A. Inspection of the Effect of Voltage Sag on EVFCS

The simulation study is carried out as follows: The total simulation time is 0.8 s, the battery is connected at 0.2 s, and the sag duration is from 0.4 to 0.6 s. Different characteristics of sag effecting EVFCS are exhibited in Fig. 9. The various characteristic magnitudes of EVFCS like V_m , V_p , V_{to} , V_{dc} and I_{bat} with sag effect are tabulated in Table V, in which 0 to 0.2 s is the no-load duration, 0.2 to 0.4 s and 0.6 to 0.8 s are the load durations without sag, and 0.4 to 0.6 s is the load duration with sag impact. The mains supply voltage (V_m) is 230 V, as exhibited in Fig. 9(a). When a heavy load is switched-ON, sag is created in the PCC voltage (V_p) and it is reduced to 115 V as

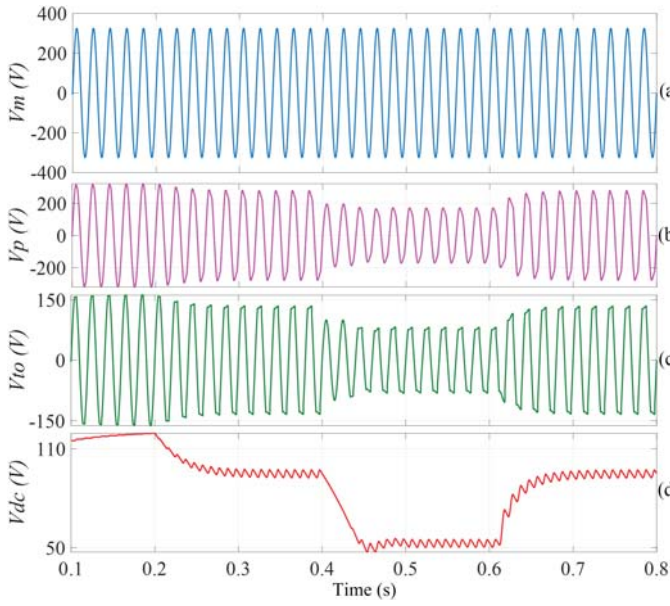


Fig. 9. Sag effected EVFCS (a) mains voltage- V_m (b) PCC voltage- V_p (c) output voltage of transformer- V_{to} (V_{ri}) (d) DC-bus voltage- V_{dc} .

TABLE V
MAGNITUDE ANALYSIS WITH SAG EFFECT

	(0 – .2) s	(.2 – .4) s	(.4 – .6) s	(.6 – .8) s
V_m (V)	230.0	230.0	230.0	230.0
V_p (V)	230.0	210.0	115.0	210.0
V_{to} (V)	110	100.4	55.0	100.4
V_{dc} (V)	110	101.0	56.4	101.0
I_{bat} (A)	0	4.94	3.0	4.94

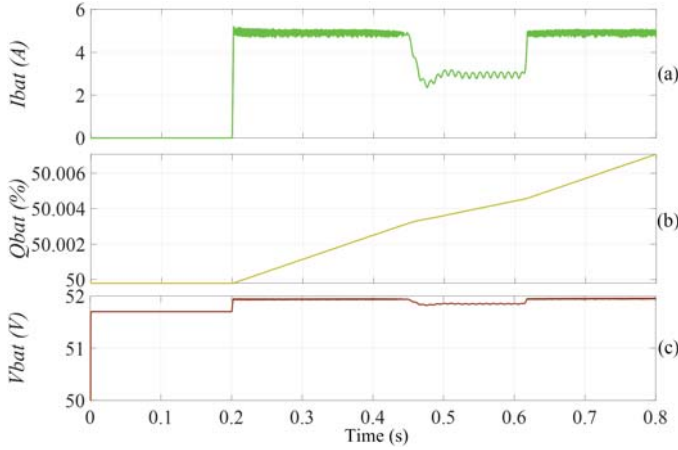


Fig. 10. Sag effected EV battery characteristics (a) battery current- I_{bat} , (b) %SOC- Q_{bat} , (c) battery voltage- V_{bat} .

depicted in Fig. 9(b). This PCC voltage sag results in a dip in the rectifier input voltage (V_{ri}). Therefore, it is reduced to 55.0 V, as exhibited in Fig. 9(c). This sagacious rectifier input voltage causes a dip in the rectifier output voltage, which is reduced to 56.4 V during the sag period, as depicted in Fig. 9(d).

Fig. 10 resembles the sag effected EV battery characteristics. The dip in the buck input voltage (V_{dc}) causes the battery to

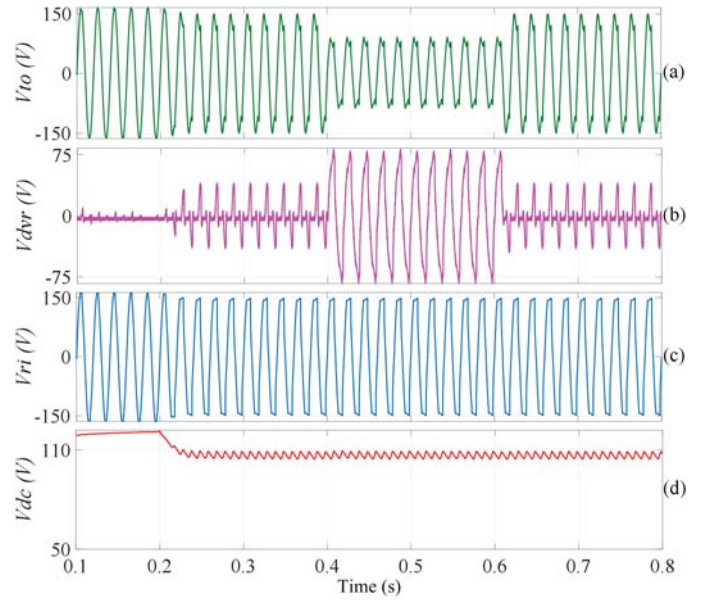


Fig. 11. Sag mitigated EVFCS characteristics, (a) output of transformer- V_{to} (b) DVR voltage- V_{dvr} (c) input of rectifier- V_{ri} (d) DC-bus voltage- V_{dc} .

TABLE VI
MAGNITUDE ANALYSIS WITH DVR MITIGATION

	(0 – .2) s	(.2 – .4) s	(.4 – .6) s	(.6 – .8) s
V_{to} (V)	110	100.4	55.0	100.4
V_{dvr} (V)	2.22	10.1	54.1	10.1
V_{ri} (V)	110	109	108	109
V_{dc} (V)	110	110	109	110
I_{bat} (A)	0	5.0	5.0	5.0

take a reduced current (I_{bat}) of 3.0 A during the sag period as exhibited in Fig. 10(a). This further causes SOC increment with a lesser rate as depicted in Fig. 10(b), which results in a longer charging time. The lithium-ion battery should take 0.42 s for 0.006% SOC increment with $C/2$ -rate, but it is taking almost 0.52 s (0.2 to 0.72 s) due to voltage sag as exhibited in Fig. 10(b). The buck output voltage (V_{bat}) is 51.95 V when there is no sag and 51.75 V during the sag period, as depicted in Fig. 10(c). Moreover, to eliminate this issue, DVR is used in EVFCS for sag mitigation in the following subsection.

B. Alleviation of Voltage Sag by DVR in EVFCS

The different characteristics of sag alleviated EVFCS are exhibited in Fig. 11. The various characteristic magnitudes of EVFCS like V_{to} , V_{dvr} , V_{ri} , V_{dc} , and I_{bat} with DVR compensation are tabulated in Table VI. The transformer output voltage (V_{to}) decreasing to 55.0 V and the injected DVR voltage (V_{dvr}) of 54.1 V during the sag period are exhibited in Fig. 11(a) and (b) respectively. Also, the DVR injected a lesser voltage of 10.1 V from 0.2 to 0.4 s and 0.6 to 0.8 s, during which a voltage drop occurred because of the EV loading condition. Since, the input voltage of rectifier (V_{ri}) is the sum of the transformer output voltage (V_{to}) and the injected DVR voltage (V_{dvr}), it is maintained sag free as exhibited in Fig. 11(c). This leads to the

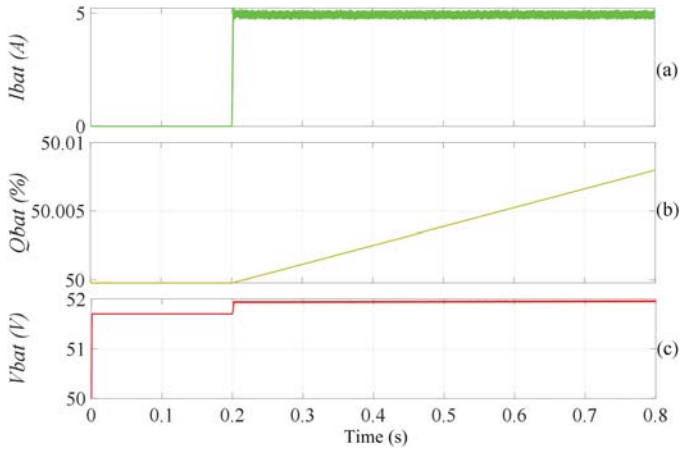


Fig. 12. Sag mitigated EV battery characteristics (a) battery current- I_{bat} , (b) %SOC- Q_{bat} , (c) battery voltage- V_{bat} .

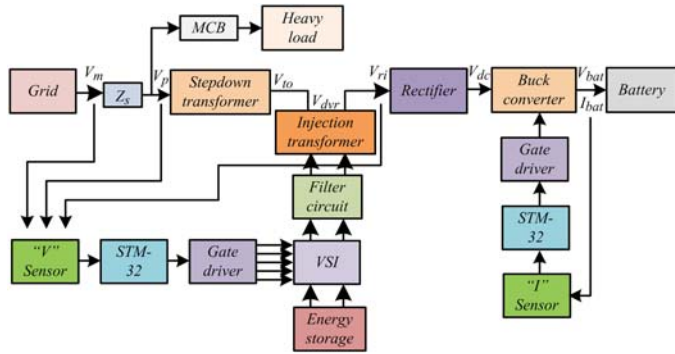


Fig. 13. Block diagram of grid fed EVFCS with DVR.

DC-bus voltage (V_{dc}) being maintained constant as shown in Fig. 11(d).

Fig. 12 exhibits the sag alleviated EV battery characteristics. The rated DC-bus voltage (V_{dc}) causes the EV battery to take current (I_{bat}) of 5.0 A, as exhibited in Fig. 12(a). This rated battery current causes SOC to increase from 50% to 50.006% in 0.42 s (0.2 to 0.62 s) only as observed in Fig. 12(b) and the corresponding sag alleviated battery voltage (V_{bat}) is exhibited in Fig. 12(c). Further, to strengthen the simulation results, an experimental study is also carried out in the following section.

VII. EXPERIMENTAL STUDY ON EVFCS

A. Experimental Investigation of the Effect of Voltage Sag

Fig. 13 shows the block diagram of grid fed EVFCS with DVR. In which the battery current is given as input to the current sensor and its output is given to the ADC of the STM32 microcontroller. The pulse generated by STM32 is given to the MOSFET switch (IRFP460 N) of the buck converter through the gate driver circuit. Similarly, the various voltages (V_m , V_p , V_{ri}) are given as inputs to the voltage sensor, and its output is given as an input to the STM32. The pulses generated by STM32 are given to the IGBT switches (FGA25N120) of VSI through

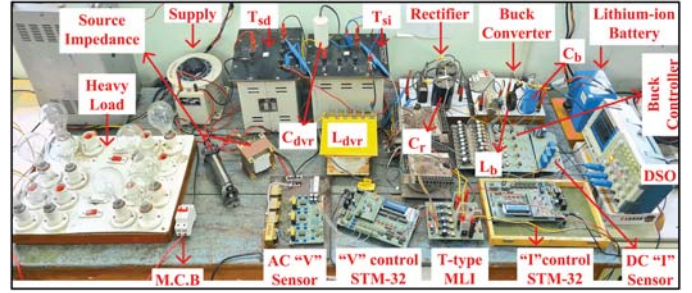


Fig. 14. Hardware implementation of EVFCS with DVR.

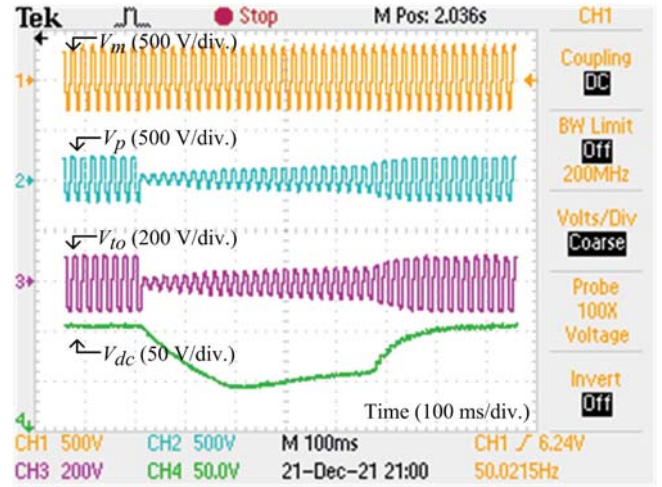


Fig. 15. Sag effected EVFCS (Ch1) mains voltage- V_m (Ch2) PCC voltage- V_p (Ch3) output of transformer- V_{to} (V_{ri}) (Ch4) DC-bus voltage- V_{dc} .

the gate driver circuit. Further, Fig. 14 shows the hardware implementation of EVFCS along with DVR. Further more, Fig. 15 resembles the hardware results of sag effecting EVFCS. In which the mains supply voltage (V_m) is 230 V, as observed in channel-1. The sag created PCC voltage (V_p) is captured in channel-2, this causes sag in the transformer output voltage (V_{to}) as observed in channel-3. Lastly, channel-4 shows the sag effected DC-bus voltage (V_{dc}).

Fig. 16 resembles the experimental results of sag effected EV battery characteristics. Firstly, the current drawn by the battery (I_{bat}) is reduced during the sag period, as captured in channel-1. This leads to the SOC characteristic increasing with the exact rate of slope-1 when there is no sag and with a lower rate of slope-2 during the sag period, as shown in channel-2. The sag effected battery voltage (V_{bat}) is observed in channel-3. Moreover, to solve this issue, DVR is used in real time study for mitigation of voltage sag in the following subsection.

B. Mitigation of Voltage Sag Experimentally Using DVR

Fig. 17 resembles the dynamic performance of DVR during the sag period. Firstly, the transformer output voltage (V_{to}) is spotted in channel-1. In channel-2, V_{dvr} is captured. This DVR injection voltage makes the V_{ri} sag free (110 V) as shown in channel-3 and further causes the constant DC-bus voltage (V_{dc})

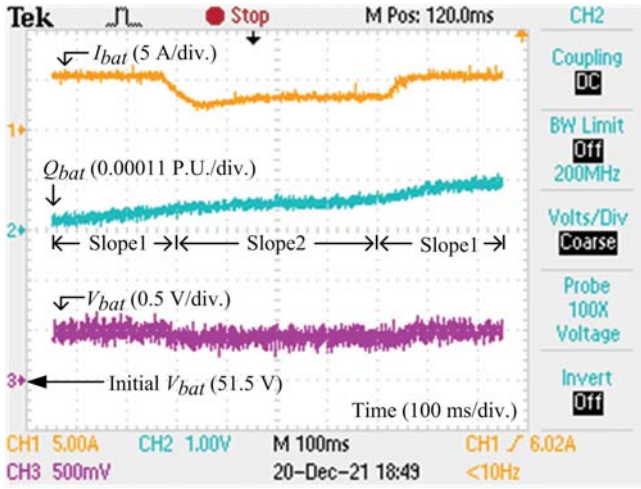


Fig. 16. Sag effected EV battery characteristics (Ch1) battery current- I_{bat} (Ch2) SOC- Q_{bat} (Ch3) battery voltage- V_{bat} .

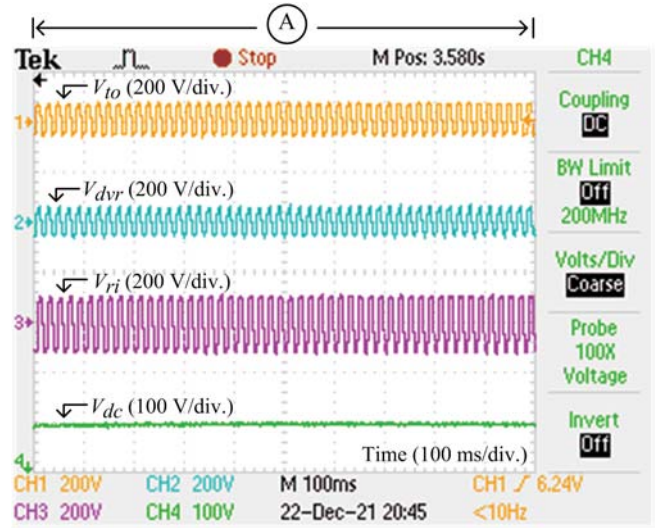


Fig. 18. Sag mitigated EVFCS (Ch1) output voltage of transformer- V_{to} (Ch2) DVR voltage- V_{dvr} (Ch3) input of rectifier- V_{ri} (Ch4) DC-bus voltage- V_{dc} .

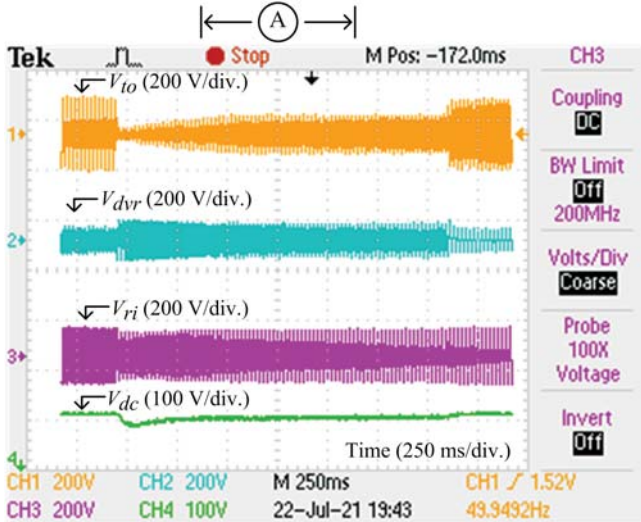


Fig. 17. Sag mitigated EVFCS (Ch1) output of transformer- V_{to} (Ch2) DVR voltage- V_{dvr} (Ch3) rectifier input voltage- V_{ri} (Ch4) DC-bus voltage- V_{dc} .

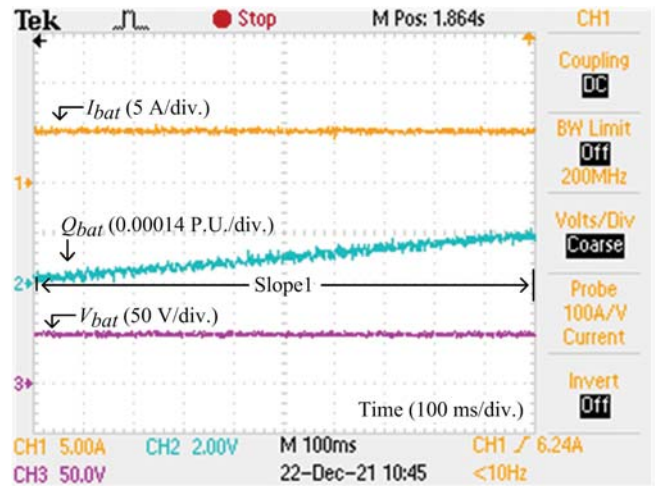


Fig. 19. Sag mitigated EV battery characteristics (Ch1) battery current- I_{bat} (Ch2) SOC- Q_{bat} (Ch3) battery voltage- V_{bat} .

to be maintained nearer to 110 V as captured in channel-4. Next, Fig. 18 resembles the steady state response of DVR, mitigating voltage sag on EVFCS.

Fig. 19 shows the sag alleviated hardware results of an EV battery. The rated DC-bus voltage causes the battery to draw a constant current (I_{bat}) of 5 A, as captured in channel-1. This constant current causes an increment of SOC at the exact rate of slope-1 as captured in channel-2. Channel-3 exhibits the sag alleviated voltage characteristic of an EV battery (V_{bat}).

The comparison of different mitigating schemes for EVFCS is tabulated in Table VII. From the comparison, it is identified that DVR can mitigate severe voltage sag of 50%.

VIII. HARMONIC STUDY ON EVFCS

The EVFCS produces voltage harmonics due to the charging of the EV battery through the working of power electronic

TABLE VII

COMPARISON OF MITIGATING SCHEMES

Compensator	Sag level (%)	System condition
Buck-converter	25	Stable
	50	Unstable
DVR	50	Stable

devices like rectifiers and buck converters. The DVR can also inject compensating voltage harmonics out of phase with harmonics generated by EVFCS, resulting in harmonic-free voltage being maintained at PCC. Fig. 20 shows the experimental results of EVFCS with harmonic mitigation using DVR. The battery load causes harmonics in the rectifier input voltage (V_{ri}) with a THD of 9.8%, shown in channel-1 and the PCC voltage THD remains the same at 9.8% without harmonic mitigation. Whereas, harmonic voltage (V_{dvr}) is injected with DVR mitigation as depicted in channel-2. This makes the PCC voltage (V_p) more

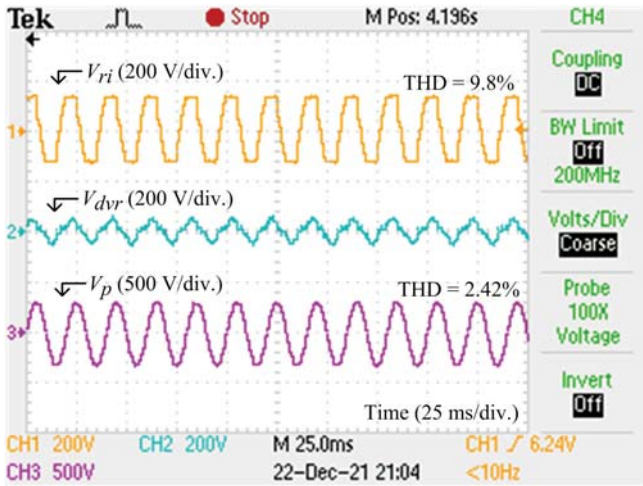


Fig. 20. Characteristics of EVFCS with harmonics mitigation, (Ch1) rectifier input voltage- V_{ri} (Ch2) DVR injected voltage- V_{dvr} (Ch3) PCC voltage- V_p .

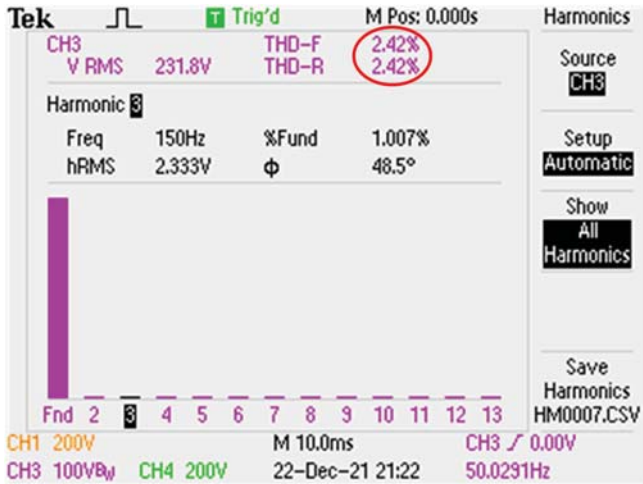


Fig. 21. THD analysis of PCC voltage- V_p .

sinusoidal, as captured in channel-3 and the THD of the PCC voltage (V_p) is maintained at 2.42% as shown in Fig. 21.

IX. RESULTS AND DISCUSSION

The comparison of DC-bus voltage (V_{dc}) with the sag effect and with DVR mitigation is demonstrated in Fig. 22. The sagacious rectifier input voltage causes a dip in the rectifier output voltage, reduced to 56.4 V during the sag period. Whereas, the sag free rectifier input voltage causes the DC-bus voltage (V_{dc}) to be maintained constant at 110 V with DVR mitigation.

The comparison of battery current (I_{bat}) with sag effect and with DVR mitigation is demonstrated in Fig. 23. The dip in the DC-bus voltage (V_{dc}) causes the battery to take reduced current (I_{bat}) of 3.0 A during the sag period; but with DVR mitigation, the constant DC-bus voltage (V_{dc}) causes the EV battery to draw current (I_{bat}) of 5.0 A.

The comparison of the charge of the battery (Q_{bat}) with the sag effect and with DVR mitigation is demonstrated in Fig. 24.

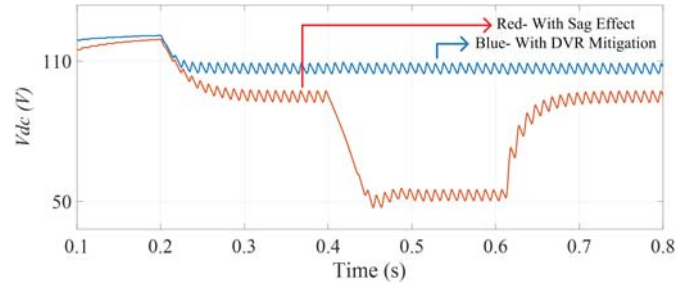


Fig. 22. DC-bus voltage- V_{dc} with sag effect (Red) and with DVR mitigation (Blue).

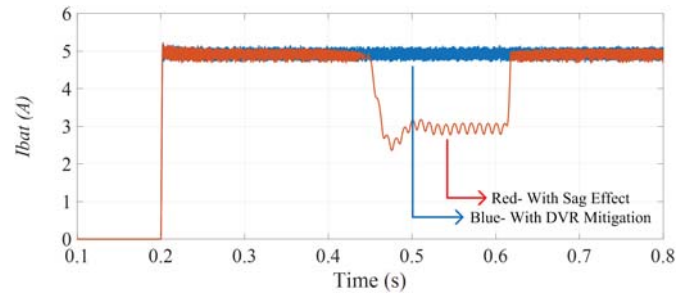


Fig. 23. Battery current- I_{bat} with sag effect (Red) and with DVR mitigation (Blue).

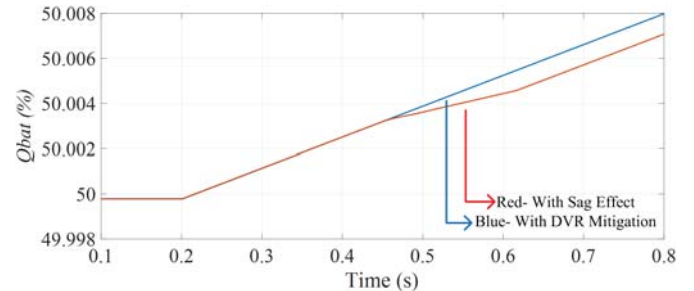


Fig. 24. Charge of the battery- Q_{bat} with sag effect (Red) and with DVR mitigation (Blue).

The sag effected battery current causes the SOC to increment at a lower rate. Actually, the lithium-ion battery should take 0.42 s for 0.006% SOC increment with $C/2$ -rate, but it is taking almost 0.52 s due to voltage sag. Whereas, it is observed that the constant battery current causes the SOC increment from 50% to 50.006% in 0.42 s only, as shown with DVR mitigation.

Further, for a severe voltage sag of 50%, the duty cycle is adjusted to 95% through the closed-loop current control strategy as shown in Fig. 25. Although the buck converter fails to maintain rated battery current as shown in Fig. 23. Whereas, the duty cycle is adjusted to 50% as shown in Fig. 25 and maintains the rated battery current of 5 A as shown in Fig. 23, with DVR mitigation.

The comparison of battery voltage (V_{bat}) with sag effect and with DVR mitigation is demonstrated in Fig. 26. The battery voltage is 51.95 V when there is no sag and 51.75 V with sag effect; but with DVR mitigation, the sag alleviated battery

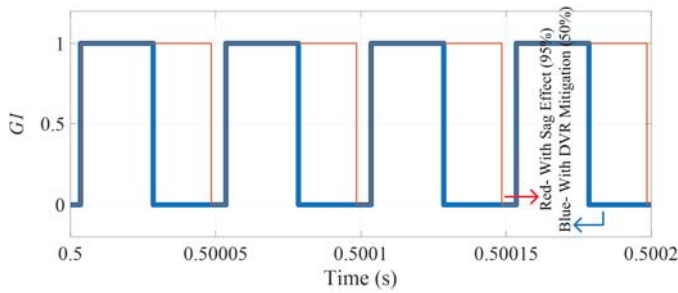


Fig. 25. Gate pulse of buck converter- G_1 with sag effect (Red) and with DVR mitigation (Blue).

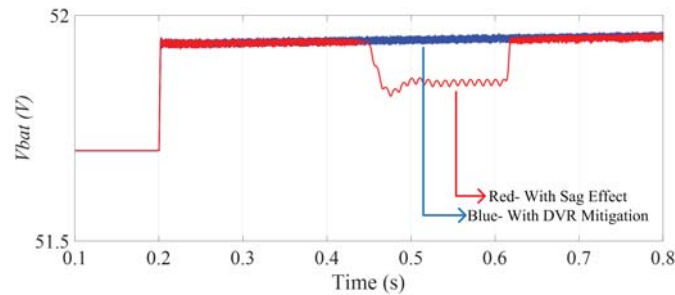


Fig. 26. Battery voltage- V_{bat} with sag effect (Red) and with DVR mitigation (Blue).

TABLE VIII
COMPARISON OF PARAMETERS

	Without/ With DVR	(0 - .2)s	(.2 - .4)s	(.4 - .6)s	(.6 - .8)s
V_{ri} (V)	Without	110	100.4	55.0	100.4
	With	110	109	108	109
V_{dc} (V)	Without	110	101.0	56.4	101.0
	With	110	110	109	110
I_{bat} (A)	Without	0	4.94	3.0	4.94
	With	0	5.0	5.0	5.0

voltage (V_{bat}) is maintained at 51.95 V during the sag duration as well.

The comparison of important parameters like rectifier input voltage (V_{ri}), DC-bus voltage (V_{dc}), battery current (I_{bat}) is tabulated in the Table VIII, without DVR and with DVR mitigation technique.

X. CONCLUSION

This manuscript demonstrated the effect of voltage sag on grid fed EVFCS and sag mitigation using a T-type 5-level DVR. Additionally, voltage harmonic elimination and battery protection are also carried out in this work. The protection of the EV battery is achieved by employing current and charge control in the buck converter. Its performance under different percentages of sag conditions is studied on the hardware platform. From the results, it is observed that the system condition is stable for 25% voltage sag. Whereas, for severe voltage sag of 50%, the buck converter is not able to maintain rated current, which results in changing SOC and battery voltage. Therefore, for mitigating severe voltage sag, a T-type 5-level inverter based DVR is used

in this research work. Further, the $\alpha\beta$ to dq transformation based 1- ϕ controller is employed for T-type 5-level DVR in this work. From the simulation and hardware results, it is identified that DVR can maintain the rated DC-bus voltage (110 V), thereby the battery current (5 A) and SOC for a severe voltage sag of 50%. In this work, the DVR is designed to compensate for a maximum voltage sag of 50%, beyond which the DVR rating and cost increase. Perhaps voltage sag occurs normally up to 50% in a practical system. Also, using the DVR mitigation technique, the PCC (grid) is protected from voltage harmonics introduced by EVFCS. The THD of PCC voltage is reduced from 9.8% to 2.42% and maintained within the IEEE 519 limit. Lastly, DVR is one of the finest devices that can mitigate voltage sag, swell, voltage harmonics, and power factor correction. However, the DVR's failure to mitigate current harmonics is its major shortcoming. The extension of this article may include power factor correction on EVFCS using DVR in the future.

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